

sufficiently small to allow reach-through breakdown in said trench DMOS transistor to occur across said epitaxial layer.

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25. A trench DMOS transistor cell as in Claim 1, wherein said trench comprises polysilicon isolated from said source and body regions by a layer of gate oxide.

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26. A trench DMOS transistor cell as in Claim 21, wherein said gate oxide having a thickness sufficient to cause semiconductor breakdown to occur at a ~~point~~ ^{location} closer to said first ~~point~~ ^{location} than said second ~~point~~ ^{location}.

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27. A semiconductor wafer comprising a predetermined number of trench DMOS transistor cells in an closed cell configuration, each trench DMOS transistor cell in said semiconductor wafer being a DMOS trench transistor cell as recited in Claim 17.

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28. A semiconductor wafer comprising a predetermined number of trench DMOS transistor cells in an open cell configuration, each trench DMOS transistor cell in said semiconductor wafer being a DMOS trench transistor cell as recited in Claim 17.

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29. A trench DMOS transistor cell as in Claim 17, wherein said substrate has a dopant concentration higher than the dopant concentration of said epitaxial layer outside of said body and source regions, said substrate and said epitaxial layer forming respectively drain and drift regions of said trench DMOS transistor cell.

Remarks

Claims 1-16 are cancelled. Applicants added Claims 17-29 to further define Applicants' invention.

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Claims 17-29 are believed allowable over the prior art of record. Therefore, early allowance of these claims are requested. If the Examiner deems a discussion over the telephone helpful to facilitate allowance of these claims, the Examiner is invited to call the undersigned Attorney for Applicants at 408-283-1222.

Respectfully submitted,

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